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Applicant: Richard A. Blanchard GROUP 110
 Assignee: Siliconix incorporated
 Title: "METHOD FOR MAKING PLANAR VERTICAL CHANNEL DMOS STRUCTURES"
 Serial No.: 06/843,454 Filing Date: 03/24/86
 Examiner: G. Ozaki Art Unit: 114
 Batch No.: G76 Date Notice of Allowability Mailed: 02/16/88
 Attorney Docket No.: M-300 US

ISSNO. 35

AUG 09 1988

Santa Clara, California
 July 29, 1988

COMMISSIONER OF PATENTS & TRADEMARKS
 Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to rule 37 CFR 1.56, Applicant brings to the Examiner's attention French Patent 2,438,342, European Patent 0,159,663, and an article entitled "A New Injection Suppression Structure for Conductivity Modulated Power MOSFETs" by Ueda et al. These references were cited in the European Search Report * of a corresponding European patent application.

Also included in the search report was an annex listing other foreign patent documents corresponding to the patents cited by the European Examiner. A copy of this annex is enclosed.

Applicant did not bring these references to the Examiner's attention earlier because Applicant received these references on July 28, 1988. Applicant attaches hereto a copy of the European Search Report. The Search Report sets forth those portions of the cited references which the European Examiner considered worth noting.

The Search Report also cites U.S. Patent 4,455,740, European Patent 0,164,095, and an article entitled "A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance" by Ueda et al., which are not included herewith because they are already of record.

Applicant requests that the above references be made of record in the present U.S. patent application.

Respectfully submitted,

Kenneth E. Leeds

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to, Commissioner of Patents and Trademarks, Washington, D.C. 20231, July 29
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Date of Signature

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